Remarks

Reconsideration and withdrawal of the outstanding art rejections in view of this submission is respectfully requested.

By the amendments presented hereinabove, previously pending claims 1, 4, 5, 8, 25, 28, 29, 31 and 33 were amended to further define the invention. Namely, in each of those claims, the featured "reaction barrier layer" was amended to read instead as metal nitride layer. The metal nitride layer of the stacked gate electrode arrangement featured in the present invention is described in connection with the example embodiment such as with regard to the metal nitride layer 105 in Figs. 1D, 2D, 3D as well as the metal nitride layer 308 in each of the gate electrodes associated with a CMOS arrangement such as shown in Figs. 5C and 7C, although not limited thereto.

According to the outstanding further non-final Office Action, all of the examined claims, namely, claims 1-8 and 17-40, were rejected under 35 USC §102(e) as anticipated by Weimer et al (US 6,291,868). It will be shown, hereinbelow, the invention claimed was neither disclosed nor suggested by Weimer et al's disclosure. Therefore, insofar as presently applicable, the outstanding art rejections of the claims are traversed and reconsideration and withdrawal of the same is respectfully requested.

The invention covers a semiconductor device scheme with one or more MOS transistors including MOS transistors with regard to a CMOS structure. Namely, according to claims 1+ and 25+, the invention calls for a semiconductor device scheme in which the gate electrode of a MOS transistor or of a CMOS transistor structure is featured as a stacked structure including a silicon layer, a metal silicide layer, a metal nitride layer and a metallic layer, formed in that order beginning with

the silicon layer. The semiconductor device scheme according to claims 5+ and 29+ similarly call for a stacked gate electrode construction such as that shown by the disclosed embodiments of the present application, although not limited thereto. Claims 33+ call for a semiconductor device comprising, on a substrate, one or more MOS transistors, each of which has a gate electrode structured similarly as that called for with regard to independent claims 1 and 5. The dependent claims further characterize the construction of the gate electrode associated with a MOS transistor or that pertaining to gate electrodes of complementary MOS transistors associated with a CMOS transistor construction. With regard to the first three disclosed examples of the present application, namely, Figs. 1E, 2D and 3D, the stacked arrangement including layers 103, 108, 105 and 106, in that order, relate to the gate electrode of the invention and with regard to the fourth and fifth disclosed example embodiments of Figs. 5C and 7C, respectively, the gate electrode stacked layers 311 (312), 320, 308 and 307, in that order, are related thereto (although not limited thereto). It is submitted, such a scheme as that defined according to claims 1+, 5+, 25+, 28+ and 33+ was, clearly, neither taught nor suggested by Weimer et al.

It is alleged, in the rejections, that Weimer et al disclosed a MOS transistor gate scheme, applicable for individual MOS transistors as well as with regard to a CMOS transistor construction, having a stacking arrangement of four layers such as that called for by the present invention. It will be shown, hereinbelow, that Weimer et al's stacked gate electrode construction is not the same as that called for according to the present claimed subject matter. This will become clearly evident in connection with the following discussion of the rejections directed to each of the separate claim groups.

I. **Rejection of Claims 1-4 and 17-21, under 35 USC §102(e), over Weimer et al.**

It is alleged that Weimer [et al] "*discloses a semiconductor device with an MOS transistor, wherein a gate electrode of the MOS transistor is provided as a stacked structure comprising a silicon layer 104, a metal silicide layer (Col. 4, lines 25-29), a reaction barrier layer 102 (Col. 3, lines 14-15), and a metallic layer 100 (Col. 3, lines 52-54)*". However, as explained in column 4, lines 25-29, in Weimer et al, the formation of metal silicide barrier layers relates to the formation of the barrier layer 102 itself and, it is submitted, does not involve an additional layer to that of the barrier layer 102 of Weimer et al. That is, Weimer et al taught a scheme including a vertically stacked gate electrode structure (e.g., 112, in Fig. 1) composed of only three (3) electrically conductive layers, namely, 100, 102 and 104. (Col. 2, lines 58-60, in Weimer et al.) Layer 116 in Fig. 1 of Weimer et al is an insulating cap layer.

As noted above, the stacked gate electrode construction such as shown in Fig. 1 of Weimer et al contains three (3) layers (i.e., silicon layer 104, barrier layer 102 and metallic layer 100). Such, it is submitted, is in clear contradistinction with that presently called for. From the discussion in column 3, lines 14-15, barrier layer 102, according to Weimer et al, is formed of material that includes metal silicide, metal nitride or metal silicide nitride, and so forth. The barrier layer in the stacked gate electrode represents one (1) layer which can be formed from any of these materials discussed in column 3, line 14+. That is, these materials are discussed, in Weimer et al, as materials that may be used in an alternative sense in connection with the formation of the barrier layer 102. This is also supported by the discussion, for example, in column 3, lines 32-33, which states that "[m]etal silicide, nitrides or silicide nitrides also have other desirable properties, etc., as well as the discussion in

column 3, lines 37-39 and that in column 4, lines 30-31. That is, Weimer et al neither disclosed nor considered a scheme featuring both the formation of a metal silicide layer and a metal nitride layer as separately formed layers in a stacking arrangement, such as that presently called for. Also, according to Weimer et al, the top most conductive layer 100 of the gate electrode stacked construction "can be made from low resistivity metals, e.g., metal or metal silicides" (see column 3, lines 52-53). That is, according to Weimer et al, a metal silicide layer is not limited to the metal silicide barrier layer 102.

According to Weimer et al, subsequent to the formation of the bottom conductive layer 104 to a thickness of 100-3000 Å (column 4, line 7-14), the barrier layer 102 is formed to a thickness of 50-500 Å, followed by heat treatment in ammonia (NH_3) or hydrazine (N_2H_4) atmosphere. Regarding the formation of the metal silicide layer, this involves first depositing a metal layer onto the bottom conductive layer 104 which is followed by a heat reaction in connection with the formation of a silicide layer. (See column 4, lines 24-30, in Weimer et al.) Once the barrier layer is formed, such as a metal silicide layer or metal nitride layer, subsequent to depositing the metal layer on the bottom layer 104, which "can include polysilicon, SiGex, or amorphous silicon, the process of annealing is performed in an atmosphere of NH_3 or N_2H_4. (Column 4, lines 31-47, in Weimer et al.)

If a metal such as tungsten (W) is deposited on the bottom layer 104 (e.g., polysilicon, SiGex, or amorphous silicon), the anneal step leads to formation of barrier layer 102 composed of, substantially, only WSi_x (tungsten silicide) and SiN (silicon nitride). This is discussed in connection with the Fig. 6 showing in Weimer et al. Weimer et al referred to their Fig. 6 illustration as a showing that the construction involves only three (3) layers, namely, a top metal tungsten (W) layer 100, an

intervening tungsten silicide nitride barrier layer (WSi_xN_y) 102 and a lowermost polysilicon conductive layer 104. (Column 4, lines 48-54.) It is submitted, Weimer et al neither disclosed nor suggested the formation of a separate metal silicide layer on a silicon layer, and the forming of a separate metal nitride layer on the metal silicide layer, followed by the forming of the uppermost metal layer on the metal nitride layer, such as that according to the present invention.

According to base claim 1 of the invention, the stacked construction includes a silicon layer, a metal silicide layer, a metal nitride layer and a metallic layer, formed in that order beginning with the silicon layer. Such four-layered stacked gate electrode construction, it is submitted, was neither disclosed nor, for that matter, suggested by Weimer et al.

In accordance with a scheme requiring the formation of a metal silicide layer inbetween the silicon layer and the metal nitride layer as that presently called for, the contact resistance effected between the metal nitride layer and the silicon layer of the resulting semiconductor device is reduced (see page 3, lines 9-13) and a desirable low contact resistance is attained between the metal silicide layer and the silicon layer (see page 12, lines 2-5, page 20, lines 13-19, and page 21, lines 5-7 of the Substitute Specification). Such was neither described nor realizable from Weimer et al's disclosure.

II. Rejection of Claims 5-8 and 22-24 under 35 USC §102(e) over Weimer et al.

It is argued, in the rejection, that the metal silicide layer of the stacked gate electrode structure "is provided on the silicon layer side and the reaction barrier layer 102 in Fig. 1 of Weimer et al is provided under the metallic layer side between the silicon layer and the metallic layer". However, as explained hereinabove, the metal

silicide layer referred to in the Office Action is, actually, the reaction barrier layer 102 in Weimer et al. That is, Weimer et al neither disclosed nor schemed a gate electrode stacked layer construction composed of forming a metal silicide layer on the lowermost silicon (polysilicon) layer, forming a metal nitride layer on the metal silicide layer, and forming an upper metal layer on the metal nitride layer. As the gate electrode structure according to claims 5+ include 4 layers, Weimer et al's disclosure teaches only a stacked gate electrode structure of only 3 layers. For the same and similar reasons as that presented hereinabove, i.e., with regard to claims 1+, the rejection of claims 5+ should also be, likewise, withdrawn.

III. Rejection of claims 25-28, under 35 USC §102(e) over Weimer et al.

It is argued in the rejection that Weimer et al disclosed a semiconductor device with complementary MOS transistors in which each of the MOS transistors features a gate electrode construction "comprising a silicon layer 104, a metal silicide layer (col. 4, lines 24-29), a reaction barrier layer 102 and a metallic layer 100, formed in that order beginning with the silicon layer as set forth in columns 3, 4 and Fig. 1." Insofar as presently applicable, it is alleged that the metal silicide layer of the invention is included in the stacked structure of the gate electrode according to Weimer et al. In that regard, Weimer et al cites the description in columns 3 and 4 as it relates to Fig. 1 illustration thereof.

The Examiner's assertion notwithstanding, the metal silicide layer in Weimer et al, it is submitted, does not represent a separate layer in the stacking arrangement to that of the reaction barrier layer 102 but, rather, is the same as that of the reaction barrier layer 102, as was shown in the above discussion in rebuttal to the rejection of claims 1+. As was shown hereinabove, the stacked gate structure of Weimer et al is

effected with only three layers. On the other hand, the present invention calls for four distinct layers in the stacking arrangement. For the same and similar reasons, therefore, the rejection of claims 25-28 is also considered improper and should accordingly be withdrawn.

IV. Rejection of Claims 29-32 and also the rejection of claims 33-40, under 35 USC §102(e), over Weimer et al.

The invention according to claims 29+ as well as that according to claims 33+ similarly call for a gate electrode construction scheme either of a MOS transistor or in connection with the complementary MOS transistors such as of a CMOS construction including a stacked arrangement including four layers such as called for in claims 1+ and 5+. Therefore, for the same and similar reasons as that argued above, the rejection of claims 29+ and 33+ is also considered improper and should accordingly be withdrawn. That is, in contradistinction with that alleged in these respective rejections, the metal silicide layer in Weimer et al's stacked structure is not a separate layer from the reaction barrier layer 102 thereof but, rather, relates to the formed reaction barrier layer 102 itself. This is because, as was shown hereinabove, the stacked structure according to Weimer et al calls for only three layers such as layers 104, 102 and 100 with regard to the gate electrode 112 construction. The barrier layer 102 therein is in the form of either a metal silicide layer, a metal nitride layer, or a metal silicide nitride layer.

Therefore, in view of the amendments presented hereinabove together with these accompanying remarks, reconsideration and withdrawal of the outstanding art rejections as well as a favorable action therefor on all of the presently pending claims, i.e., claims 1-8 and 17-40, and an early formal Notification of Allowability of the above-identified application is respectfully requested.

A marked-up version showing changes made is enclosed herewith.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (500.40010X00), and please credit any excess fees to such deposit account.

Respectfully submitted,
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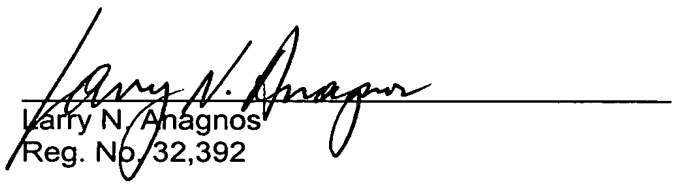

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MARKED-UP VERSION SHOWING CHANGES MADE

IN THE CLAIMS:

Please **amend** claims 1, 4, 5, 8, 25, 28, 29, 31 and 33 as follows:

1. (Twice Amended) A semiconductor device with an MOS transistor, wherein a gate electrode of the MOS transistor is provided as a stacked structure comprising a silicon layer, a metal silicide layer, a ~~reaction barrier~~ metal nitride layer and a metallic layer, formed in that order beginning with the silicon layer.

4. (Amended) A semiconductor device according to Claim 1, wherein the metal silicide layer is a tungsten silicide layer, the ~~reaction barrier~~ metal nitride layer is a tungsten nitride layer, and the metallic layer is a tungsten layer.

5. (Twice Amended) A semiconductor device with an MOS transistor whose gate electrode is provided as a stacked structure comprising a silicon layer and a metallic layer as the uppermost layer thereof, wherein a metal silicide layer is provided on the silicon layer side and a ~~reaction barrier~~ metal nitride layer is provided under the metallic layer side between the silicon layer and the metallic layer.

8. (Amended) A semiconductor device according to Claim 5, wherein the metal silicide layer is a tungsten silicide layer, the ~~reaction barrier~~ metal nitride layer is a tungsten nitride layer and the metallic layer is a tungsten layer.

25. (Amended) A semiconductor device with complementary MOS transistors, each MOS transistor having a gate electrode, a source region and a

drain region, wherein the gate electrode is provided as a stacked structure comprising a silicon layer, a metal silicide layer, a ~~reaction barrier~~ metal nitride layer and a metallic layer, formed in that order beginning with the silicon layer.

28. (Amended) A semiconductor device according to claim 25, wherein the metal silicide layer is a tungsten silicide layer, the ~~reaction barrier~~ metal nitride layer is a tungsten nitride layer, and the metallic layer is a tungsten layer.

29. (Amended) A semiconductor device with complementary MOS transistors, each MOS transistor having a gate electrode, a source region and a drain region, wherein the gate electrode is provided as a stacked structure comprising a silicon layer, an uppermost metallic layer, a metal silicide layer provided on the silicon layer side and a ~~reaction barrier~~ metal nitride layer provided under the metallic layer side between the silicon layer and the metallic layer.

31. (Amended) A semiconductor device according to claim 29, wherein the metal silicide layer is a tungsten silicide layer, the ~~reaction barrier~~ metal nitride layer is a tungsten nitride layer, and the metallic layer is a tungsten layer.

33. (Amended) A semiconductor device comprising on a substrate, at least one MOS transistor, wherein a gate electrode of the MOS transistor is provided as a stacked structure comprising a silicon layer, a metal silicide layer, a ~~reaction barrier~~ metal nitride layer and a metallic layer, formed in that order beginning with the silicon layer.